AQA A-LEVEL PHYSICS · 7408

PHYSICS



EXAM QUESTION PACK

3.13 ELECTRONICS: CAPACITOR CIRCUITS

SCORE	PERCENTAGE
/31	%

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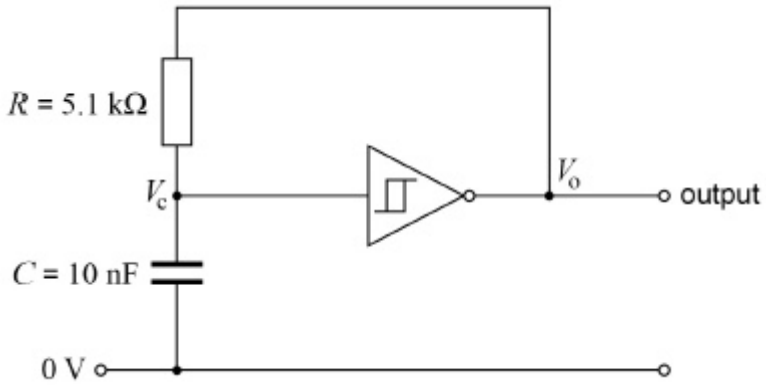
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Q1.

(a) **Figure 1** shows an astable circuit based on a NOT logic gate. The symbol in the centre of the logic gate means that the output V_o changes at two different input values of V_c depending on whether the input voltage is rising or falling.

Figure 1



The pulse repetition frequency (PRF) for this particular circuit is given by:

$$\frac{1}{1.4\,RC}$$

Calculate the PRF in kHz

PRF = _____ kHz

(1)

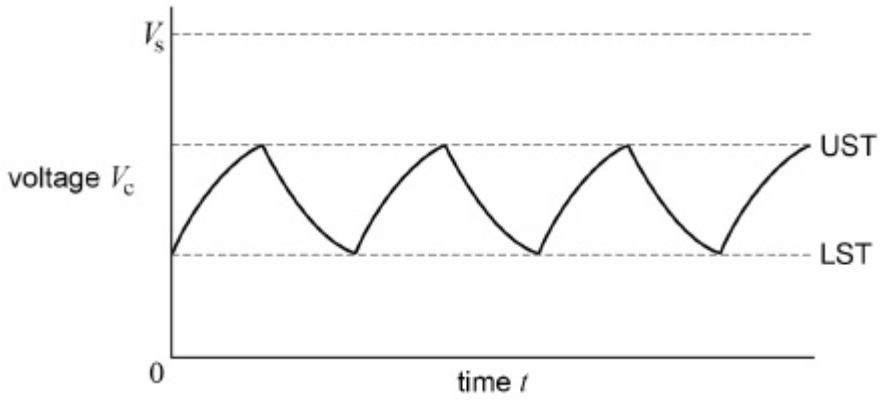
(b) The supply voltage to the NOT gate is V_s

- When V_c increases and reaches the upper switching threshold (UST), the output of the NOT gate will switch from V_s to 0 V
- When V_c decreases and reaches the lower switching threshold (LST), the output of the NOT gate will switch from 0 V to V_s

The graph in **Figure 2** shows V_c constantly changing as the capacitor charges and discharges.

Figure 2

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Draw on **Figure 2** the output voltage V_o for the astable circuit.

(1)

(c) The circuit in **Figure 1** can be modified by the addition of a resistor to vary the PRF.

The astable is to be modified so that it produces a frequency 4 times that of the original.

Calculate the value of the resistor that should be added to the circuit and explain where in the circuit this additional resistor should be placed.

value of resistor = _____ kΩ

_____

_____

_____

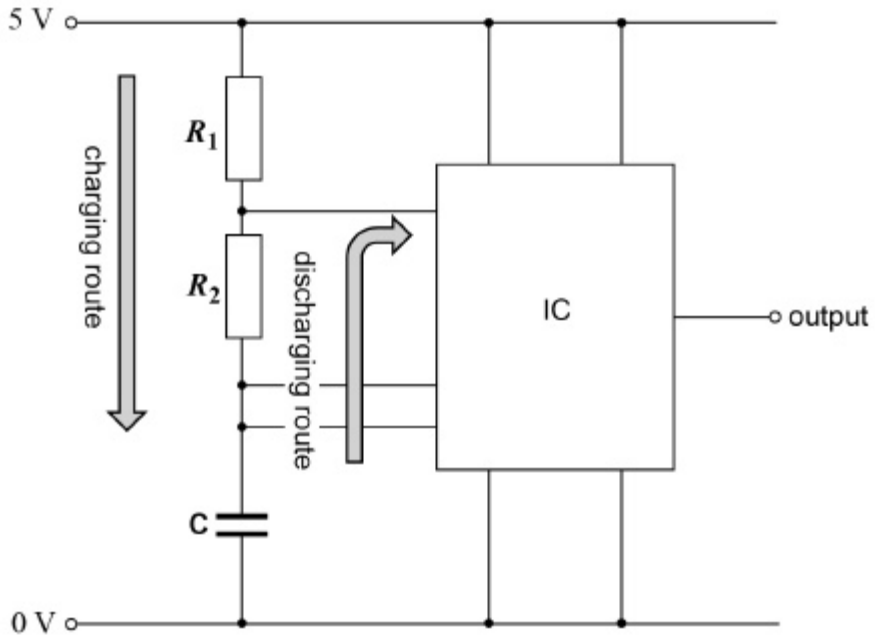
_____

(2)

(d) In another astable, two resistors (R_1 and R_2) and a capacitor **C** form a timing chain to control the mark and space times for a square wave produced at the output of the integrated circuit (IC) shown in **Figure 3**.

Figure 3

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The charging time for the capacitor **C** is: $t_C = 0.7 \times (R_1 + R_2) \times C$

The discharging time for the capacitor **C** is: $t_D = 0.7 \times R_2 \times C$

Calculate, in kΩ, values for $\boldsymbol{R_1}$ and $\boldsymbol{R_2}$ needed to produce a 5 kHz signal with 75% duty cycle given that the capacitor **C** has a value of 10 nF

$\boldsymbol{R_1}$ = _____ kΩ

$\boldsymbol{R_2}$ = _____ kΩ

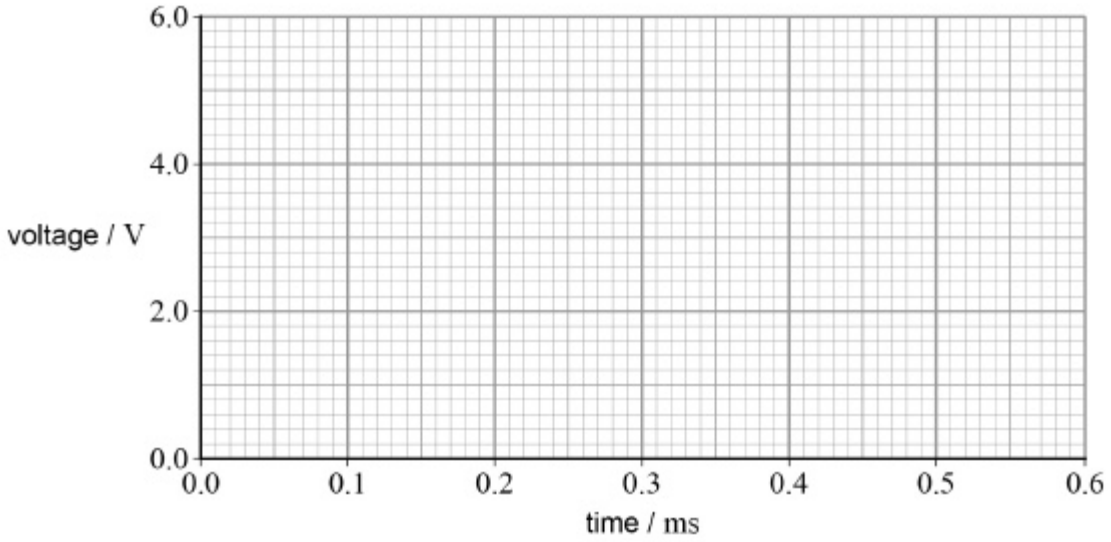
(2)

(e) The output of the IC in **Figure 3** is 5 V during the charging period and 0 V during the discharging period.

Draw on **Figure 4** the wave pattern that represents this signal.

Figure 4

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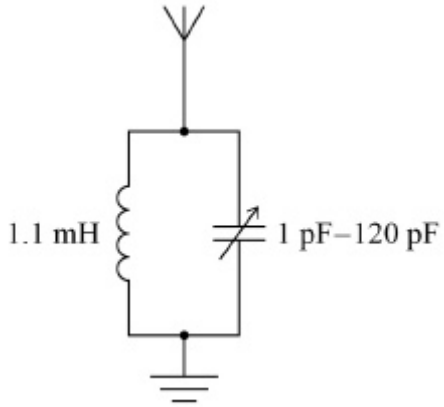
(2)

(Total 8 marks)

Q2.

Figure 1 shows the first-stage filter circuit for a simple AM receiver. The circuit can be adjusted to resonate at 910 kHz so that it can receive a particular radio station.

Figure 1



(a) Calculate the value of the capacitance when the circuit resonates at a frequency of 910 kHz.

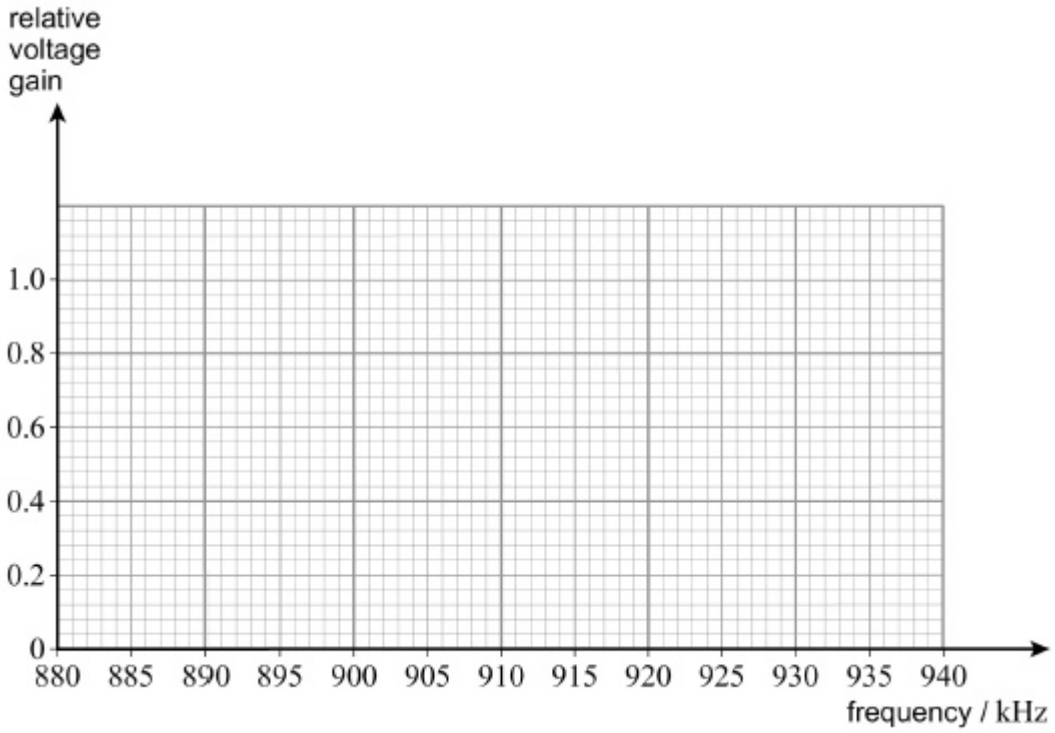
capacitance = _____ pF

(2)

(b) Draw on **Figure 2** an ideal response curve for the resonant circuit, labelling all relevant frequency values based upon a 10 kHz bandwidth.

Figure 2

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(3)

(c) The *Q*-factor for the practical tuning circuit has a smaller value than the ideal one assumed in question (b).

Discuss the changes the listener might notice when tuning to this station due to the practical *Q*-factor being smaller.

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(2)

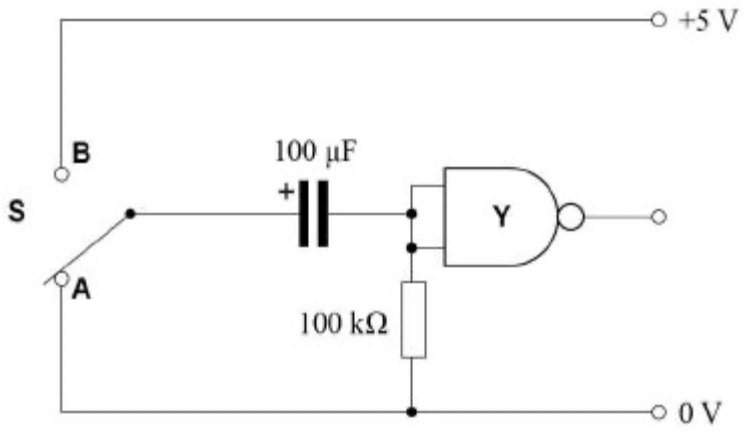
(Total 7 marks)

Q3.

A student experiments with the circuit shown in **Figure 1**.

Figure 1

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Y is a NAND gate for which an input of less than 2.5 V is logic state 0 and input greater than 2.5 V is logic state 1.

Switch **S** is set to position **A** for a long time so that the capacitor is uncharged.

(a) Explain why the output of **Y** is logic state 1.

_____

_____

_____

(1)

(b) When **S** is moved to position **B**, the capacitor charges through the 100 kΩ resistor.

Show that the capacitor will be charged to 2.5 V after about 7 s.

(2)

(c) Suggest an application for a circuit such as that shown in **Figure 1**.

_____

_____

_____

(1)

(Total 4 marks)

Q21.

In order to reduce the bandwidth needed for transmission of an audio speech signal, the signal is filtered to remove high frequencies.

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(a) Explain what is meant by the **bandwidth** of a signal.

_____

_____

_____

(2)

(b) Name the type of filter needed to remove high frequencies.

_____

(1)

(c) (i) Draw the circuit diagram of a passive filter to remove high frequencies, using a resistor and a capacitor.

Label the input and the output.

(2)

(ii) The resistor in the filter has a value of 1 kΩ.

Calculate the capacitor value required to give a breakpoint frequency of 4.0 kHz.

_____

_____

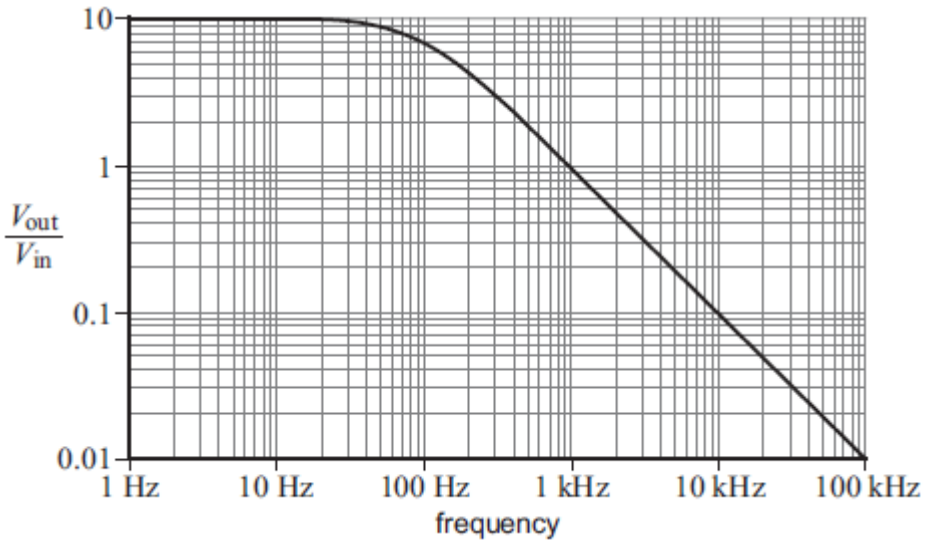
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(3)

(d) The graph shows the response of a different filter to remove high frequencies.

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(i) State how the graph shows that this must be an **active** filter.

_____

(1)

(ii) Circle the value closest to the breakpoint frequency of this filter.

30 Hz 100 Hz 200 Hz 1 kHz

(1)

(iii) A 2 V, 5 kHz signal is applied to the input of this filter.

Calculate the output signal voltage.

_____

_____

(2)

(Total 12 marks)

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